periods of data access activity, said [power] variable voltage [supplied] being less during said periods of no data access activity [being less] than [said power supplied] during said periods of data access activity, whereby power consumption of said memory integrated circuit is curtailed.

18. (Twice amended) The dynamic power management device of Claim 2, wherein said periods of data access activity include memory access periods and memory refresh periods, wherein said periods of no data access activity include standby periods including periods between refresh periods and wherein said logic control means causes said power control means to supply to said integrated circuit a relatively low value of said voltage during [a] said standby [period] periods, a higher value of said voltage during said memory refresh periods, and a still higher value of said voltage during said memory access periods.

22. (Amended) The integrated circuit of Claim [19] 21, wherein said logic control means causes said memory integrated circuit to enter said first, second or third operation period only when said power control means supplies a voltage meeting the voltage requirements of said memory integrated circuit to enter said first, second or third operation period, respectively.

23. (Twice amended) A dynamic power management device for supplying power to a solid state memory integrated circuit in a computer system having a power source supplying a substantially constant voltage, said dynamic power management device comprising:

power control means coupled to said power source for supplying a variable voltage to said memory integrated

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circuit, said variable voltage being less than or equal to said substantially constant voltage supplied by said power source; and

logic control means for generating address and control signals for said memory integrated circuit and for controlling said power control means to supply power to said memory integrated circuit at a level to maintain memory information in said memory integrated circuit during periods of no data access activity and to supply power at a level to read and write memory information in said memory integrated circuit during periods of data access activity, said power supplied during periods of no data access activity being less than said power supplied during periods of data access activity, said variable voltage being less during periods of no data access activity than during periods of data access activity, whereby power consumption of said memory integrated circuit is curtailed.

REMARKS

Under 35 U.S.C. § 112, first paragraph, the Examiner objected to the specification as failing to give an enabling disclosure and rejected claims 1-20 and 22.

Claim 1 is amended in part by deleting the words "without varying a voltage being supplied to elements of said electronic system other than said memory integrated circuit". Claim 22 is amended to depend from Claim 21 rather than from Claim 19. It is respectfully requested, based on the amendments of claims 1 and 22, that the rejection of Claim 1 and dependent claims 2-20 and of Claim 22 be withdrawn.

The Examiner rejected claims 1-23 under U.S.35 § 102(b) as being clearly anticipated by Dias et al. The rejection is respectfully traversed.

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